Master of Technology in **Embedded Systems**
Department of Electronics & Communication Engineering
Draft for approval

Subject Code	Course Title	Credit Total(L T P)
Semester 1 (Core Courses)		
ECT701	Data structures & algorithms	3 (3-0-0)
ECT702	Advanced microcomputer systems & interfacing	3 (3-0-0)
ECT631	Digital System Design & FPGAs	3 (3-0-0)
ECT703	CAD Algorithms for Synthesis of VLSI Systems	3 (3-0-0)
ECT990	Mathematical Methods & Techniques for ECE technologists-I*	3 (3-0-0)
ECP709	Hardware systems Lab	2 (0-0-4)
ECP711	Software systems lab	2 (0-0-4)
	Total Semester Credits	19
Semester 2 (2 + 5 electives)		
ECP612	System Design lab	3 (0-0-6)
ECD656	Minor Project	4 (0-0-8)
	(Elective Courses)#	
ECT702	Advanced Embedded software design	3 (3-0-0)
ECT704	Computer vision	3 (3-0-0)
ECT614	Advance Computer Architecture	3 (3-0-0)
ECT690	Wireless Sensor Networks	3 (3-0-0)
ECT616	Computer Arithmetic & Micro-architecture Design	3 (3-0-0)
ECT618	Graph Algorithms & Combinatorial optimization	3 (3-0-0)
ECT622	System Level Design & Modeling	3 (3-0-0)
ECT624	VLSI Testing & Testability	3 (3-0-0)
ECT626	Formal Verification of Digital Hardware & Embedded Software	3 (3-0-0)
ECT628	Memory design & testing	3 (3-0-0)
CPTxxx	Parallel & distributed systems	3 (3-0-0)
ECT632	Embedded systems	3 (3-0-0)
ECT634	Micro-& Nano- electro-mechanical Systems (MEMS & NEMS)	3 (3-0-0)
ECT638	Design of Asynchronous Sequential Circuits	3 (3-0-0)
ECT642	FPGAs Physical Design	3 (3-0-0)
ECT654	RF Integrated Circuits	3 (3-0-0)
ECT656	Adaptive Signal Processing	3 (2-0-2)
ECT657	VLSI signal processing architectures	3 (2-0-2)
ECT***	RF MEMS	3 (3-0-0)
ECT662	Advanced Digital Signal & Image Processing	3 (3-0-0)
	Total Semester Credits	22
Semester 3		
ECD659	Dissertation	16(0 0 32)
	Total Semester Credits	16
Semester 4		
ECD660	Dissertation	16(0 0 32)
	Total Semester Credits	16
	Total Credits of all semesters	73

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#These courses will be offered by the faculty of Department.
#The students may opt for any of the elective course offered in the Institute on recommendation of supervisor
* only one course out of ECT990 or ECT992 shall be offered and ONLY one is required to be opted.
***to be floated and numbered

PG Course Details

Program: *M. Tech. (Embedded Systems)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT-701	**Course Name:** Data Structures & Algorithms
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Overview of Data Structures: Review of Arrays, Stacks, Queues, linked lists , Linked stacks and Linked queues, Applications
Algorithm Analysis: Efficiency of algorithms, Apriori Analysis, Asymptotic Notations, Time complexity of an algorithm using O notation, Polynomial Vs Exponential Algorithms, Average, Best, and Worst Case Complexities, Analyzing Recursive Programs.
Trees and Graphs: Introduction, Definition and Basic terminologies of trees and binary trees, Representation of trees and Binary trees, Binary tree Traversals, Threaded binary trees, Graphs-basic concepts, representation and traversals. Binary Search Trees, AVL Trees and B Trees: Introduction, Binary Search Trees: Definition, Operations and applications. AVL Trees: Definition, Operations and applications. B Trees: Definition, Operations and applications.
Red – Black Trees: Splay Trees and Hash Tables, Red – Black Trees, Splay Trees and its applications. Hash Tables: Introduction, Hash Tables, Hash Functions and its applications.
Divide – and – Conquer & Greedy Method: General Method, Binary Search, Finding Maximum and Minimum, Quick Sort, Merge sort, Strassen's; Matrix Multiplication, Greedy Method- General Method, Minimum Cost Spanning Trees, Single; Source Shortest Path.
Dynamic Programming: General Method, All Pairs Shortest Path, Single Source Shortest Path, 0 / 1 Knapsack problem, Reliability Design, Traveling Sales Person's Problem.
Back Tracking and Branch – and – Bound: General Method, 8 – Queen's Problem, Graph Coloring. Branch – and – Bound: The Method, LC Search, Control Abstraction, Bounding, 0 / 1 Knapsack Problem.

Text/ Refernces:

1. Mark Allen Weiss, ―Data Structures and Algorithm Analysis in C++‖, Pearson
2. Education, 2002.
3. Kruse R.L., Data Structure and Program Design, PHI.
4. Data structures and Algorithms in C++, Michael T.Goodrich, R.Tamassia and Mount, Wiley student edition, John Wiley and Sons.
5. Rivest, Cormen, Introduction to Algorithms, MIT Press
6. Ellis Horowitz, Sartaj Sahni, Fundamentals of Data Structures
7. Aaron M. Tenenbaum, Y. Langsam, Moshe J. Augenstein, Data Structures Using C

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Program: *M. Tech. (Embedded Systems)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT-702	**Course Name:** Embedded Micro computer Systems & Interfacing
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

- Introduction;
- Design of software- assembly language, layered software systems, device drivers, object oriented interfacing, Threads and recursion debugging, semaphores, thread scheduling;
- Interfacing methods- protocols, synchronization, parallel I/O, serial I/O;
- Interrupt Synchronization & Timing generation- Features of interrupts, interrupt vectors & priority, polling, priority algorithms; frequency measurement, frequency and period conversion.
- Serial and parallel port interfaces;
- State machine & concurrent process models.
- System examples- camera etc.
- Selected topics- Memory interfacing, high speed I/O interfacing, Analog interfacing, data acquisition systems, simple networks (SCI port, CAN, I^2C, X-10, USB).

References

1. Jonathan W. Valvano, Embedded Microcomputer Systems: Real-Time Interfacing, Brookes/Cole, Pacific Grove, 2000.
2. F. Vahid & T. Givargis, Embedded System Design, Wiley.
3. Wolf, W., Computers as Components: Principles of Embedded Computing System Design, Morgan Kaufmann, San Francisco, 2001.
4. Furber, S., ARM: system-on-chip architecture, 2nd Edition, Addison-Wesley, London, 2000.
5. Hayes, J. P., Computer Architecture and Organization, 3rd Edition,, McGraw-Hill

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Program: *M. Tech. (Embedded Systems)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT703	Course Name: CAD Algorithms for Synthesis of VLSI Systems
Credit: 3	L-T-P: 2-1-0
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Role of CAD in digital system design, levels of design, modeling & description and support of languages, RTL, gate and system level synthesis; Technological alternatives and technology mapping;

CAD tools for synthesis, optimization, simulation and verification of design at various levels as well as for special realizations and structure such as microprogrammes, PLAs, gate arrays etc. Low power issues in high level synthesis and logic synthesis.

Circuit partitioning, placement and routing algorithms. Circuit Compaction; Deep sub-micron issues; interconnects modeling and synthesis.

Books:

1. G. D. Micheli. Synthesis and optimization of digital systems.
2. Dutt, N. D. and Gajski, D. D. High level synthesis, Kluwer, 2000.
3. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.
4. N. Deo, Graph Theory, PH India.
5. Introduction to VLSI Physical Design flow. Circuit partitioning, placement and routing algorithms. Design Rule-verification, Circuit Compaction; Circuit Extraction and post layout simulation.
6. FPGA design flow- partitioning, placement and routing algorithms.
7. Deep sub-micron issues; interconnects modeling and synthesis.
8. Sait, S. M. and Youssef, H. VLSI Physical design automation. IEEE press, 1995.
9. Sherwani, N. VLSI physical design automation. Kluwer, 1999.
10. Sarrafzadeh, M. and Wong, C. K. An introduction to VLSI physical design, Mc Graw Hill, 1996.
11. Brown, S. D., Francis, R. J., Rose, J. and Vranesic, Z G. Field programmable Gate arrays. Kluwer, 1992.
12. Betz, V., Rose, J. and Marquardt, A. Architecture and CAD for Deep-submicron FPGAs. Kluwer, 1999.
13. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.

Program: *M. Tech. (Embedded Systems)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT990	Course Name: Mathematical Methods and techniques for Electronics & Communication Technologists-I
Credit: 3	L-T-P: 2-1-0
Pre-requisite course:	
Co-requisite course:	

Syllabus:

[The following contents have implicit application to and exemplification through ECE problems such as communication over unreliable channel, processing of random signals, amplitude modulation by random signals, reliability of a electronic/communication systems, resource sharing in a system, and networks of queues]

A. Applied Probability and probability models: one- and two-dimensional random variables (RVs); discrete RVs- Poisson, geometric, binomial, hyper-geometric & multi-model; continuous RVs- normal, exponential, Gamma, chi-square, bivariate normal; moment generating function & Laplace of RV distribution; Random processes; Markov chain- continuous, discrete; Poisson process; renewal theory; queuing theory; reliability theory; 16 Hrs.

B. Brownian motion & stationery processes; Computer methods for generating RVs; Simulation- general & special techniques for continuous and discrete distributions, multi-variate distributions; variance reduction techniques; Monte-Carlo techniques 05 Hrs.

C. Transforms & systems analysis- Fourier Series, Fourier transform, z-transform, discre cosine (sine) transform, Wavelet transform, fractional transforms. 07 Hrs.

Suggested references (not limited to)-

1. Probability, random variables and stochastic processes, A. Papoulis and U. S. Pillai, Mc Graw Hill.
2. Probability & random processes for Electrical Engineers- Alberto Leon Garcia, Pearson (I)Applied Probability models for optimization- Sheldon M. Ross, Elsevier, 2009
3. Mathematical methods in Electrical engineering, Thomas B. A. Senior, Cambridge University Press

Further references

1. Discrete Wavelet transforms, Patrick J. Van Fleet, Wiley Interscience, 2007
2. Probability & statistics for engineers & scientists- Sheldon M. Ross, Elsevier, 2009
3. PROBABILITY AND STATISTICS IN ENGINEERING, William W. Hines, Douglas C. Montgomery, David M. Goldman. Connie M. Borror, John Wiley & Sons, 2008
4. Laplace and Fourier transforms for electrical engineers, Edward J. Craig, Holt, Rinehart and Winston, 1964
5. Computational Probability- Winfried K. Grassman, Kluwer

Program: ***M. Tech. (Embedded Systems)***	**Department:** ***Electronics & Comm. Engg.***
Course Code: ECT 992	**Course Name: Mathematical Methods and techniques for Electronics & Communication Technologists-II**
Credit: 3	**L-T-P: 2-1-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

[The following contents implicit application to and exemplification through ECE problems such as reduced order polynomials, order reduction of a transfer function, sparse matrix based solution of large systems, implementation of search algorithms for design space exploration]

A. Linear algebra and Matrix analysis – Groups, fields and rings; vector spaces; basis & dimensions; canonical forms; inner product spaces- orthogonalization, Gram-Schmidt orthogonalization, unitary operators, change of orthonormal basis, diagonalization; eigenvalues & eigen vectors- Gerschgorin theorem, iterative method, Sturm sequence, QR method, introduction to large eigen value problems. 10 Hrs.
B. Function approximation & reduced order modelling of systems- Taylor's polynomial, least square approximation, Chebyshev series/polynomial, splines, Pade & rational approximation, Krylov subspaces, Lanczos process, Arnoldi method; Symbolic analysis and reduced order modelling of interconnects, linear and weakly non-linear analog/digital systems 12 Hrs.
C. Combinatorial optimization- counting methods, algorithms for optimization 06 Hrs.

Suggested references (not limited to)-

1. Topics in Algebra, I. N. Herstein, Wiley. Theory and Applications of Numerical Analysis, G. M. Phillips, Peter J. Taylor, Academic press
2. Advanced Model Order Reduction Techniques in VLSI Design, Sheldon Tan, Lei He, Cambridge Univ. Press, 2007.
3. Model Order Reduction: Theory, Research Aspects and Applications edited by W. H. A. Schilders, Henk A. Van Der Vorst, Joost Rommes, Springer.
4. Combinatorial optimization, Papadimitriou and Steiglitz, PHI (I)

Further references

1. MODEL ORDER REDUCTION TECHNIQUES WITH APPLICATIONS IN ELECTRICAL ENGINEERING, Luigi FORTUNA, Guiseppe NUNNARI, Antonio GALLO, Springer, 1992.
2. Y. Saad, Numerical methods for large Eigenvalue problems, www.umn.edu
3. Matrix Analysis & linear algebra, Meyer, SIAM
4. Schaum's outline on Linear Algebra, McGraw Hill
5. H. A. van der Vorst, Iterative methods for large linear systems, citeseerx.ist.psu.edu
6. Cheng et al, Symbolic analysis and reductions of VLSI circuits, Springer, 2005

Program: ***M. Tech. (Embedded Systems)***	**Department:** ***Electronics & Comm. Engg.***
Course Code: ECP-709	**Course Name:** Hardware Systems Lab
Credit: 2	**L-T-P: 0-0-4**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Problem-set for algorithm implementation:

Boolean algebraic formulations

a. Covering algorithm- Brach & bound
b. ROBDD computation
c. Operation between ROBDDs: '+', '.'

Graph based optimization

a. Two consideration each
b. Two consideration each
c. Graph coloring
d. Clique partitioning
e. Edge covering
f. Vertex covering
g. Independent set finding

List scheduling

a. Latency constrained resource minimization
b. Resource constrained latency minimization
c. Path based scheduling
d. Pipelined data-path scheduling
e. Hu's multiprocessor scheduling

Allocation & binding

a. FU binding
    a. Coloring
    b. Clique finding
    c. Left edge based binding
b. Storage unit binding
    a. Coloring
    b. Clique finding
    c. Left edge based binding
c. Interconnect binding
    a. Coloring
    b. Clique finding

edge based binding

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Program: *M. Tech. (Embedded Systems)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECP-711	**Course Name:** Software Systems Lab
Credit: 2	**L-T-P: 0-0-4**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

- Design of software-
  - assembly language programming
  - device drivers writing
  - object oriented interfacing,
  - debugging

- Interfacing methods
- Analog interfacing, data acquisition systems (board based)

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Program: ***M. Tech. (Embedded Systems)***	**Department:** ***Electronics & Comm. Engg.***
Course Code: ECT-605	**Course Name:** Digital System Design & FPGAs
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Sequential Logic Design- Introduction, Basic Bistable Memory Devices, additional bistable devices, reduced characteristics and excitatio table for bistable devices.

Synchronous Sequential Logic Circuit Design- Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronou sequential design of Moore, Melay Machines,

Algorithmic State Machine- An Algorithm with inputs, digital solution, Implementation of traffic light controller, ASM charts, Desig Procedure for ASMs.

Data path and Control design.

Introduction to VHDL/Verilog- Data types, Concurrent statements, sequential statements, behavioral modeling.

Introduction to programmable logic devices- PALs, PLDs, CPLDs and FPGAs.

FPGA mapping of combinational & sequential designs

Books:

1. Digital System Design, Ercegovac, Wiley.
2. Richard S. Sandige, *Modern Digital Design,* McGraw-Hill, 1990.
3. Zvi Kohavi, Switching and Finite Automata Theory, Tata McGraw-Hill.
4. Navabi. Analysis and modeling of digital systems. McGraw Hill, 1998.
5. Perry. Modeling with VHDL. McGraw Hill, 1994.
6. Navabi. Verilog Digital Design. McGraw Hill, 2007.

Program electives-

Program: ***M. Tech. (Embedded Systems)***	**Department:** ***Electronics & Comm. Engg.***
Course Code: ECP-702	**Course Name:** Advanced Embedded Software Design
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Processor micro-architecture, application-specific architecture, Embedded OS, middleware, graphics libraries, Software Development Tools, graphics IPs, virtual prototyping solutions, RTOS, Embedded linux, concurrency & concurrent programming languages; Design automation of such systems including methodologies, techniques and tools for their design as well as novel designs of software components.

References:

1. Short, K, *Embedded Microprocessor System Design*, Prentice Hall, 1998.
2. Embedded Linux, Pearson
3. Edward A. Lee, "Embedded Software", Advances in Computers (M. Zelkowitz, editor) 56, Academic Press, London, 2002.
4. Testing Embedded Software, by Bart Broekman and Edwin Notenboom, Pearson/Addison-Wesley (UK), ISBN: 0-321-15986-1
5. Design Patterns for Embedded Systems in C: An Embedded Software Engineering, Bruce Powel Douglass, Newnes, Elsevier.
6. Software Engineering for Embedded Systems: Methods, Practical Techniques, Robert Oshana, Mark Kraeling, Newnes, Elsevier.
7. Embedded Software, Newnes know it all series, Jean J. Labrosse, ISSN 1879-8683, Elsevier.
8. Programming Embedded Systems in C and C++, O'Reilly Series, Michael Barr.
9. Real-Time Concepts for Embedded Systems, CMP books, R and D Developer Series, Qing Li, Caroline Yao, CRC press.
10. Linux for Embedded and Real-time Applications, Doug Abbott, Newnes, Elsevier, 2003.
11. An Embedded Software Primer, David E. Simon, Addison Wesley, 1999.
12. Testing Embedded Software, Broekman Bart, Pearson Education India, ISBN 813172509X, 9788131725092.
13. Performance Analysis of Real-Time Embedded Software, Yau-Tsun Steven Li, Sharad Malik, Kluwer.

Embedded Software for SoC, Ahmed Amine Jerraya, Springer.

PG Course Details

Program: ***M. Tech. (VLSI Design)***	**Department:** ***Electronics & Comm. Engg.***
Course Code: ECT630	**Course Name:** Advanced Computer Architecture
Credit:	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus

System Buses.
Memory systems and error detection and error correction coding.
Input/Output Modules & organization.
Operating System Support.
Instruction formats, instruction sets and their design, Pipelining.
CPU Structure & RISC Architectures.

Books:

1. D. Patterson and J. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann Publishers, Inc., Second edition, 1998.
2. Computer Architecture: A Quantitative Approach, John L. Hennessy & David A Patterson, Morgan Kaufmann, 1996.
3. Structure Computer Organization, 4th Edition, Andrew S. Tanenbaum, Prentice Hall, 1999.
4. Computer Architecture and Organization, J. Hayes, McGraw Hill, 1988.
5. Computer Organization and Architecture, 5th Edition, William Stallings, Prentice Hall, 1996.

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PG Course Details

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT704	**Course Name:** Computer Vision
Credit:	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus

Computer vision is concerned with the computation of three dimensional world from digital images- the theory behind artificial systems that extract information from images.

Other topics- feature detection, image segmentation, motion estimation, image mosaics, 3D shape reconstruction, and object recognition; image formation, processing, analysis, and interpretation; machine learning techniques; statistical approaches; sensors.

Applications areas are- image-based rendering, computer graphics, robotics, photo interpretation, image retrieval, video analysis and annotation, multi-media, and more.

Connections with human perception: computational and architectural aspects of human vision.

References:

1. Reinhard Klette (2014). Concise Computer Vision. Springer. ISBN 978-1-4471-6320-6.
2. Richard Szeliski, Computer Vision: Algorithms and Applications
3. Forsyth & Ponce, Computer Vision: A Modern Approach, Pearson, 2002, ISBN 0130851981
4. Linda G. Shapiro and George C. Stockman (2001). Computer Vision. Prentice Hall. ISBN 0-13-030796-3.
5. Tim Morris (2004). Computer Vision and Image Processing. Palgrave Macmillan. ISBN 0-333-99451-5.
6. Bernd Jähne and Horst Haußecker (2000). Computer Vision and Applications, A Guide for Students and Practitioners. Academic Press. ISBN 0-13-085198-1.
7. Milan Sonka, Vaclav Hlavac and Roger Boyle (2008). Image Processing, Analysis, and Machine Vision. Thomson. ISBN 0-495-08252-X.
8. David A. Forsyth and Jean Ponce (2003). Computer Vision, A Modern Approach. Prentice Hall. ISBN 0-13-085198-1.
9. Dana H. Ballard and Christopher M. Brown (1982). Computer Vision. Prentice Hall. ISBN 0-13-165316-4.
10. Barghout, Lauren, and Jacob Sheynin. "Real-world scene perception and perceptual organization: Lessons from Computer Vision." Journal of Vision 13.9 (2013): 709-709.
11. Turek, Fred (June 2011). "Machine Vision Fundamentals, How to Make Robots See". NASA Tech Briefs magazine 35 (6). pages 60–62
12. Steger, Carsten, Markus Ulrich, and Christian Wiedemann (2008). Machine Vision Algorithms and Applications. Weinheim: Wiley-VCH. p. 1. ISBN 978-3-527-40734-7. Retrieved 2010-11-05.

E. Roy Davies (2005). Machine Vision: Theory, Algorithms, Practicalities. Morgan Kaufmann. ISBN 0-12-206093-8.

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Program: M.Tech ECE	Department: ECE
Course Code: ECT690	Course Name: Wireless Sensor Networks
Credit:3	L-T-P: 3-0-0
Pre-requisite course:	

Syllabus:-

Network architecture, wireless communication: the physical layer in WSN, WSN medium access control and link layer protocols, WSN services: synchronization and localization, topology control and routing, data-centric and content-based routing, Quality of Service and transport protocols, in-network aggregation and WSN security

Books:

1. Murthy &Manoj, "Ad Hoc Wireless Networks: Architectures and Protocols," ISBN 0-13-147023-X, Pearson 2004
2. William Stallings, “Wireless Communications & Networks”, ISBN: 0131918354, Prentice Hall; 2nd edition, November 12, 2004.

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT-616	**Course Name:** Computer Arithmetic & Micro-architecture Design
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Computer arithmetic- conventional & higher radix number systems, residue & logarithmic number systems; sequential & parallel (and high speed) algorithms for addition, multiplication, division; evaluation of elementary functions- sin, cos, $\sin^{-1}$, $\cos^{-1}$, sinh etc; CORDIC method for trigonometric functions.languages for design description (HDLs) like VHDL or Verilog; Modeling and simulation of circuits at various levels;

Data path design for high performance- pipelining & systolic arrays; Control design- sequential, hardwired & micro-programmed control.

Topics in design-yield and redundancy,

Low power design techniques.

Books:

For Review

1. Kohavi, Switching & finite automata theory, Mc Graw Hill

Computer arithmetic

2. Ercegovac, Digital Systems, Wiely, 2004
3. Parhami, Computer Arithmetic- Algorithms & Hardware Design, Oxford Univ. Press
4. Koren, Computer Arithmetic Algebra, Prentice Hall Inc.

For Data-path/Control Design

5. Hayes, J P, Computer Architecture & organization, Mc Graw Hill, 2003

For HDLs

6. Navabi. Introduction to VHDL. Mc Graw Hill, 2000
7. Bhaskar. VHDL Primer. Prentice Hall India, 2001
8. Navabi. Verilog digital systems. Mc Graw Hill, 2000
9. Palnitkar, Verilog…., Pearson India/Prentice-Hall India

Low power design

10. Chandrakasan, A. P. Low-power design methodologies. IEEE Press, 1998.
11. Mead & Conway, VLSI circuit design
12. Raguram, R. Modeling and Simulation of Electronic circuits. PHIndia, 1996.
13. Weste and Eshraghian. Principles of CMOS VLSI design. Addison Wesley, 1998.
14. K. Roy and et al, Low power design, Wiley

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT-624	**Course Name:** VLSI Testing &Testability
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Physical Faults and their modeling; Stuck at Faults, Bridging Faults; Fault collapsing; Fault Simulation: Deductive, Parallel, and Concurrent Fault Simulation. Critical Path Tracing;

ATPG for Combinational Circuits: D-Algorithm, Boolean Differences, PODEM Random, Deterministic and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage.

PLA Testing, Cross Point Fault Model and Test Generation.

Memory Testing- Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests; Delay Faults.

ATPG for Sequential Circuits: Time Frame Expansion ; Controllability and Observability Scan Design, BILBO , Boundary Scan for Board Level Testing ; BIST and Totally self checking circuits.

System Level Diagnosis & repair- Introduction; Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes.

Reconfiguration Techniques; Yield Modeling, Reliability and effective area utilization.

Books:

1. Abramovici, M., Breuer, M. A. and Friedman, A. D. Digital systems testing and testable design. IEEE press (Indian edition available through Jayco Publishing house), 2001.
2. Bushnell and Agarwal, V. D. VLSI Testing. Kluwer.
3. Agarwal, V. D. and Seth, S. C. Test generation for VLSI chips. IEEE computer society press.
4. Hurst, S. L. VLSI testing: Digital and mixed analog/digital techniques. INSPEC/IEE, 1999.

PG Course Details

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: EV-622	**Course Name:** System Level Design & Modeling
Credit:3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

System level design, description languages- SystemC, SDL, SpecChart etc.
Hardware-software codesign- partitioning, interface synthesis, case studies. Application specific processors, Retargetable compilers, instruction set-simulation and co-simulation.
Architectural synthesis for DSP applications.
Formal Verification of digital hardware systems- BDD based approaches, functional equivalence, finite state automata, automata, FSM verification. Model checking.

Books:

1. Gajski, Gupta and Vahid, Specifications and design of Embedded systems
2. Topics on formal verification to be covered using topics from literature.

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PG Course Details

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT-626	**Course Name:** Formal Verification of Digital Hardware & Embedded Software
Credit:3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Formal Verification of digital hardware systems- BDD based approaches, functional equivalence, finite state automata, -automata, FSM verification. Model checking; various industry & academia CAD tools for formal verification.
Verification, validation & testing - Debugging techniques for embedded software, instruction set simulators, clear box technique, black box testing, evaluating function test,

Books:

1. Embedded systems Design- Artist Roadmap for Research & Development, LNCS-3436, Springer.
2. J. W. Valvano, Eembedded microcomputer systems- Real Time Interfacing, , Thomson press (Cengage India)
3. Computers as components- Principles of embedded computing system design. Wolf, W., Academic Press (Indian edition available from Harcourt India Pvt. Ltd., 27M Block market, Greater Kailash II, New Delhi-110 048.)
4. Verification, validation & testing in software engineering, A. Dasso and A. Funes, Idea Group Inc.
5. Advanced Formal Verification, R. Drechsler, Kluwer.
6. Hardware-Software codesign for data flow dominated embedded systems, R. Niemann, Springer.
7. Readings in Hardware/Software codesign, Micheli, Ernst, Wolf, Morgan Kaufmann.

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PG Course Details

Program: ***M. Tech. (VLSI Design)***	**Department:** ***Electronics & Comm. Engg.***
Course Code: ECT628	**Course Name:** Memory Design & Testing
Credit:3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Processing technology for Memories: Multipoly Floating Gate and Control Gate, Trench Capacitors and thin Oxide.
Memory Modeling and testing faults in SRAMs, Marching Tests; Delay Faults.
Semiconductor memory architecture, Space of memory faults- fault primitives.
Preparation of Circuit Simulation: Definition & location of open, short, and bridge fault, Simulation methodology.
Test for single cell and two port SRAMs, Functional fault modeling and testing of RAMS,
Fault Diagnosis & Repair Algorithms.
Built –in self Test and design for testabiltity of RAMs.
Built in self repair architecture.
Trend in Embedded Memory testing.

Books:

1. Pinaki Mazumder, Kanad Chakraborty, Testing and Testable Design of High-Density Random-Access Memories (Frontiers in Electronic Testing), Kluwer academic pub.
2. Said Hamdioui, Testing Static Random Access Memories: Defects, Fault Models and Test Patterns (Frontiers in Electronic Testing), Kluwer academic pub 2004.
3. Pinaki Mazumder and Kanad Chakraborty, Fault –Tolerence and reliability techniques for High –Density Random-Acess Memories, Pearson India, 2002.

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PG Course Details

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECP612	**Course Name:** System Design Lab
Credit:3	**L-T-P: 0-0-6**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

S. No	*Objective Of Experiment*
A-1	Layout Design- (i) Full adder, D-FF ; & (ii) synthesis of combinational & Sequential Components- 4-bit adder, 4-bit shift register, sequence detector ("1010")
A-2	Layout synthesis of already designed (1st Odd Semester) Data Path & Control for an arithmetic/logic application. Synthesis Using SYNOPSYS/CADENCE tool

Individual Application/Problems:
1.GCD-computer (4-bit)
2. Booth multiplier (4-bit)
3. 4-pt FFT
4. 4-pt IFFT
5. CORDIC for SinΘ/CosΘ
6. CORDIC for $Sin^{-1}Θ/Cos^{-1}Θ$
7. Non-Linear function exp(-2.5)/Sin 1.45/ Cos3.1/Sinh2.5/ Cosh3.2/log-natural
8. Find Average of Floating Point Numbers in Array of Size 16/32/64/128

1. For pseudo exhaustive TPG set T for BIST, follow the theorem concerning logical segmentation, which relates n (inputs), k (subspaces of size k among n), w (weight of n-tuple). Indicate w as well as $|T_c|$ for different c; and n=20, k=3. Take example circuits/sub-systems for implementing the scheme & generating/applying random test patterns.
2. A circuit implementing f=xy+yz is to be tested using the syndrome-test method. Show that the faults z s-a-0 and z s-a-1 are not detected, while all other single stuck-at faults are detected. Arrange for experimental setup for all such testable as well as non-testable faults.
3. In a shift register polynomial division method of compression, a type 2 LFSR with $P^*(x)=1+x^2+x^4+x^5$ is to be used for input sequence 1 1 1 1 0 1 0 1 (8 bits). Compute signature for the input sequence. Indicate at least one more input sequence, which would alias the given sequence. Arrange for experimental setup for verifying your design.

Books:

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PG Course Details

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT632	**Course Name:** Embedded Systems
Credit:3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus

Embedded computing- Microprocessors, embedded design process, system description formalisms. Instruction sets- CISC and RISC;

CPU fundamentals- programming I/Os, co-processors, supervisor mode, exceptions, memory management units and address translation, pipelining, super scalar execution, caching, CPU power consumption.

Embedded computing platform- CPU bus, memory devices, I/O devices, interfacing, designing with microprocessors, debugging techniques.

Program design and analysis- models of program, assembly and linking, compilation techniques, analysis and optimization of execution time, energy, power and size.

Processes and operating systems- multiple tasks and multiple processes, context switching, scheduling policies, inter-process communication mechanisms.

Hardware accelerators- CPUs and accelerators, accelerator system design.

Networks- distributed embedded architectures, networks for embedded systems, network-based design, Internet-enabled systems.

System design techniques- design methodologies, requirements analysis, system analysis and architecture design, quality assurance.

Books:

1. Wolf, W. Computers as components- Principles of embedded computing system design. Academic Press (Indian edition available from Harcourt India Pvt. Ltd., 27M Block market, Greater Kailash II, New Delhi-110 048.)

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PG Course Details

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT634	**Course Name:** Micro& Nano Electro Mechanical System (MEMS & NEMS)
Credit:3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus

Micro Electro Mechanical System (MEMS) Origins. MEMS Impetus / Motivation.
Material for MEMS. The toolbox: Processes for Micro machining.
MEMS Fabrication Technologies. Fundamental MEMS Device Physics: Actuation. Fundamental
MEMS Devices: The Cantilever Beam. Microwave MEMS Applications: MEM Switch Design Considerations. The Micromachine
Transmission Line. MEMS-Based Microwave Circuit and System.

Books:

1) Micro-electromechanical (MEM) Microwave Systems by Hector J.De Los Santos, Artechhouse.
2) An Introduction to Micro-electromechanical System by Nadim Maluf, Artechhouse.

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PG Course Details

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT638	**Course Name:** Design of Asynchronous Sequential Circuits
Credit:3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus

Introduction: Summary of synchronous techniques - disadvantages in today's technology. Advantages of asynchrononous techniques - low power, performance, modularity. Historic difficulties with asynchronous design. Flow Table Reduction, The state-assignment Problem, Delays, Hazards, and Analysis, Feedback, other Modes of operation, Counters.

Circuit Classification*:* Bounded Delay, speed independent, and delay independent. Data models (single-rail, dual-rail). Handshaking protocols (2 phase, 4 phase)

Micropipeline *Circuits*: Basic building blocks. Pipelines, with and without data processing elements. The design of the Amulet processors.

NCL Logic: The NULL convention logic approach. Preserving delay insensitivity, threshold gates with hysteresis.

Formal Aspects of Asynchronous: The Rainbow approach. Green descriptions of micro-pipelines. Overview of formal basis to asynchronous descriptions

Books:

1. Asynchronous sequential circuits by Stephen H. Unger, John Wiley & Sons
2. Switching and Finite Automota Theory. Kohavi, Tata McGraw Hill

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PG Course Details

Program: *M. Tech. (VLSI Design)*	**Department:** *Electronics & Comm. Engg.*
Course Code: ECT642	**Course Name:** FPGAs Physical Design
Credit:3	**L-T-P: 2-0-2**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Introduction to FPGA Architectures.
FPGA design flow, partitioning, placement and routing algorithms.
Technology mapping for FPGAs, case studies.

Books:

1. Brown, S. D., Francis, R. J., Rose, J. and Vranesic, Z G. Field programmable Gate arrays. Kluwer, 1992.
2. Betz, V., Rose, J. and Marquardt, A. Architecture and CAD for Deep-submicron FPGAs. Kluwer, 1999.
3. Trimberger, S. M. FPGA Technology. Kluwer, 1992.
4. Oldfield, J. V. and Dorf, R. C. FPGAs: Reconfigurable logic for rapid prototyping and implementation of digital systems. John Wiley, 1995

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Program: *M. Tech. (VLSI Design)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT 657 UG Code : ECT 468	Course Name: **VLSI based Signal Processing Architectures**
Credit: 3	L-T-P: 3-0-0
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Introduction for DSP algorithms : VLSI Design flow, Mapping algorithms into Architectures: Graphical representation of DSP algorithms – signal flow graph (SFG), data flow graph (DFG), critical path, dependence graph (DG). Data path synthesis, control structures, Optimization at Logic Level and architectural Design, Loop bound and iteration bound, Algorithms for computing iteration bound, Iteration bound of Multirate data-flow graphs.

Parallel and pipeline of signal processing application : Architecture for real time systems, latency and throughput related issues, clocking strategy, power conscious structures, array architectures; Pipelining processing of Digital filter, Parallel processing, Parallel and pipelining for Low power design, Optimization with regard to speed, area and power, asynchronous and low power system design, ASIC (application specific integrated circuits) and ASISP application specific instruction set processors) design;

Systolic Array Architecture: Methodology of systolic array architecture, FIR based Systolic Array, Selection of Scheduling Vector, Matrix multiplication of systolic array

Architecture of different signal processing modules : Convolution technique, Retiming concept, Folding /Unfolding Transformation, CORDIC architecture

Low power Design :Theoretical background , Scaling v/s power consumption, power analysis, Power reduction techniques, Power estimation approach

Application in communication and signal processing system: Transformation architectures, source and channel coding structures, Motion Estimation and motion compensation for video, Speech processing algorithm

Suggested references (not limited to)-

1) VLSI Digital Signal Processing Systems: Design and Implementation
By K.K. Parhi , John Wiley & Sons, 1999 (ISBN Number: 0-471-24186-5)
2) Richard J, Higgins, Digital Signal Processing in VLSI, Prentice Hall, ISBN-10: 013212887X, ISBN-13: 9780132128872
3) M.A. Bayoumi, VLSI Design Methodology for DSP Architectures, Kluwer, 1994
4) U. Meyer – Baese , Digital Signal Processing with FPGAs, Springer, 2004

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Program: *M. Tech. (VLSI Design) M. Tech. (ECE)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT 656 **UG Code : ECT 467**	**Course Name: Adaptive Signal Processing**
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite course:	
Co-requisite course:	

Syllabus:

Adaptive Filter Structures and Algorithms :

Introduction to Adaptive systems, Adaptive Linear combiner, Minimum Mean-Square Error, Wiener-Hopf Equation, Error Performance Surface, LMS algorithm, Convergence of weight vector, Learning Curve, FX-LMS algorithm (Filtered X-LMS) and its application to ANC, Types of LMS, RLS algorithm, Matrix Inverse Lemma for RLS, Computational complexity of LMS and RLS, Convergence Analysis.

Advancements in Transforms :

Short time Fourier Transform (STFT), Multi Resolution Analysis, Wavelet Transform, Continuous Wavelet Transform (CWT), Inverse CWT, Discrete Wavelet Transform, Sub-band coding and implementation of DWT, Applications (signal and image compression, de-noising, detection of discontinuous and breakdown points in signals), S-transform, Frequency selective filtering with wavelet and S-transform.

Applications:

Direct Modelling or System Identification, Inverse Adaptive Modelling (Equalization), Adaptive Noise Cancellation, Adaptive filters for time series and stock market prediction, Biomedical Applications (Cancellation of 50-Hz interference in Electro-Cardiography, Cancelling donor heart interference in heart-transplant electrocardiography, Cancelling Maternal ECG in Fetal Electrocardiography), Echo Cancellation in Long distance Telephone Circuits, Adaptive self tuning filter, Adaptive line enhancer, Adaptive filters for classification and data mining.

Suggested references (not limited to)-

[1] B. Widrow and S. D. Stearns : Adaptive Signal Processing, Prentice Hall.
[2] D. G. Manolakis, V. K. Ingle, S. M. Kogon : Statistical and Adaptive Signal Processing, McGraw Hill.
[3] S. S. Haykin : Adaptive Filter Theory, 4th Edition, Prentice Hall.
[4] A. H. Sayed : Fundamentals of Adaptive Filtering, John Wiley & Sons.
[5] H. G. Stark : Wavelets and Signal Processing, Springer.
[6] S. Mallat, A Wavelet tour of Signal Processing, Academic Press.
[7] Rabi Polikar, The wavelet Tutorial, Part I-IV, Online available by Rowan University, Glassboro, NJ 08028.
[8] R. G. Stockwell, L. Mansinha, and R. P. Lowe, Localization of the Complex Spectrum : The *S* Transform, IEEE Transactions On Signal Processing, Vol. 44, No. 4, April 1996.

View John Cabot University's current and upcoming course schedules and syllabi. Learn more about the options for studying abroad at an American university.Â Co-requisite: EN 110). Thomas Govero. TTH 1:30-2:45 PM.Â Introductory Italian I (This course carries 4 semester hours of credit, except for Summer sessions, when it carries 3 semester hours of credit.) Matilde Galante. Mw 3:00 pm 4:50 pm. IT 101-11. Introductory Italian I (This course carries 4 semester hours of credit, except for Summer sessions, when it carries 3 semester hours of credit.) Valentina Dorato. Tth 8:30 am 10:20 am. IT 101-12. Introductory Italian I (This course carries 4 semester hours of credit, except for Summer sessions, when it carries 3 semester hours of credit.) Anna Mauceri Trimnell. This course catalogue includes two types of course codes: Courses beginning with a UNYP course code are designated for the 4-year programs. Courses beginning with a BBA course code are designated for the 3-year Business program. Please see individual programâ€™s study plan to determine if and how the given course fits the program. Some courses may be required for certain programs, be electives for other programs, or fulfill general education requirements.Â General Education: Lower-Level Courses. UNYP 77217 African Politics and Society 3 semester credits Pre-requisite: None. A general introduction to the African continent and its contemporary problems. A study of the historical and political evolution and an analysis of its societies and diversity.